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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,326	LAI, BENNY W.H.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-20 remain in the application. Claims 1 and 9 have been amended. Claims 1-20 have been examined.

Response to Arguments

2. Applicant's arguments filed 09/23/2004 with respect to amended claim 1 have been considered but are moot in view of the new ground(s) of rejection.

As per arguments for amended claim 1:

The Applicant rightfully relates the USB physical layer 18 comprises a built-in self-test (TX-BIST) circuit 35, a multiplxer 36 and a built-in self-analyzer circuit 49 to the tester circuit within the SERDES. However, it was not the Examiner's intention to identify these components as the "plurality of testers", but when the USB physical layer is repeated (i.e. the two USB physical layers on page 6, ¶ 48) it became a "plurality of testers". Since the built-in self-test (TX-BIST) circuit 35, multiplxer 36 and built-in self-analyzer circuit 49 is part of a single SERDES circuit or USB physical layer 18 it would stand to reason that these components comprise a single tester circuit. The Applicant respectfully points out that "the tester as disclosed in Takinosawa [0048] is limited to only testing two chips or USB physical layers. The Examiner asserts that although Takinosawa, by way of example, discusses two chips, he certainly does not limit the illustration to only two chips. However, for the sake of argument, Takinosawa (US-2003/0035473) in view of Lesea (US-2003/0023912) suggests a plurality of SERDESs

and functionally identical testers with a FPGA that includes sixteen built-in self-test SERDES circuits that are each capable of communicating at gigabit speeds. (Page 2, ¶s 23, 25, 27). The Applicant states "that the two USB layers (or SERDESS) are completely separate and not integrated or embedded within the same integrated circuit". The Examiner would like to point out that it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate Takinosawa's USB physical layer components on the same integrated circuit, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965).

It is the Examiner's conclusion that the combination of Takinosawa in view of Lesea teaches all the limitations of amended claim 1 and, therefore, is not patentably distinct or non-obvious over the prior art of record. The new grounds of rejection for claims 1-8 follow.

3. Applicant's arguments filed 09/23/2004 with respect to amended claim 9 and original claim 15 have been fully considered but they are not persuasive.

As per arguments for amended claim 9:

The Applicant states "Takinosawa does not teach that the USB physical layer chips and the USB link layer are components of the same integrated circuit fabricated onto the same semiconductor substrate". The Applicant also states "Takinosawa does not teach that a plurality of SERDESs/testers may be integrated onto the same semiconductor substrate". The Applicant further states "Because there is no teaching in

Takinosawa regarding Integrating a plurality of SERDESs and testers onto the same semiconductor substrate, it follows that there is a plurality of FTIs and a plurality of FTCs may be integrated onto the same semiconductor substrate". The Examiner would like to point out that it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate Takinosawa's USB link physical components on the same integrated circuit fabricated onto the same semiconductor substrate, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965).

It is the Examiner's conclusion that independent claim 9 is not patentably distinct or non-obvious over the prior art of record namely, Takinosawa (US-2003/0035473). Therefore, the rejection is maintained. Based on their dependency on claim 9, claims 10-14 stand rejected.

As per arguments for claim 15:

The Applicant states "The test Interfaces and test controllers of the claimed invention are embedded within the same integrated circuit, whereas in the cited prior art, the test interfaces and test controllers exist within separate integrated circuits". The Examiner would like to point out that it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate Takinosawa's TX-BIST circuit 35 (test interface) and multiplexer 36 (test controller) included in the USB physical layer on the same integrated circuit, since it has been held that forming in one piece an article

which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965).

It is the Examiner's conclusion that independent claim 9 is not patentably distinct or non-obvious over the prior art of record namely, Takinosawa (US-2003/0035473). Therefore, the rejection is maintained. Based on their dependency on claim 15, claims 16-20 stand rejected.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 9-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Takinosawa (US-2003/0035473), hereinafter Takinosawa.

Claim 9:

Takinosawa teaches a peripheral device 10 (substrate) comprises a microcontroller 12 (core circuitry), an application layer 14, a USB link layer 16 (core circuitry) and a USB physical layer 18 (SERDESs and testers). (Page 2, ¶ 20). Takinosawa also teaches shift register 39 functions to convert the parallel data received from the bit stuffer circuit 38 into a serial data stream and shift register 46 functions to convert the serial data received as an input signal into parallel data (SERDES). (Page 3, ¶ 25 and 26). Takinosawa further teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (functional test interface (FTI)) functions to generate a series of

pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (functional test controller (FTC)). Takinosawa discloses that multiplexer 36 (functional test controller (FTC)) is controlled via the TX-BIST enable signal (select operational modes) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (functional test interface (FTI)) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2). Takinosawa further discloses that data to be transmitted is provided by the microcontoller 12 (external device) to the USB link layer 16 (input/output controller (IOC)) which functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 via a data bus 21 (common test bus) as well as transmit control signals 23 (addressable commands). (Page 2, ¶ 22).

Claim 15:

Takinosawa teaches when TX-BIST enable signal is active (enables test controllers), the TX-BIST circuit 35 (test interface) functions to generate a series of pseudo random data words (parallel data), which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (test controller). Takinosawa also teaches that multiplexer 36 (test controller) is controlled via the TX-BIST enable signal (triggering test operations) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (test interface) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2). Takinosawa also discloses it is possible to conduct self test on two chips (e.g. two USB physical layers) (plurality of test interfaces and test controllers). (Page 6, ¶ 48).

Claim 10:

Takinosawa further teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (functional test interface (FTI)) functions to generate a series of pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester controller). Takinosawa discloses that multiplexer 36 (tester controller) is controlled via the TX-BIST enable signal (select operational modes) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (tester interface) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2).

Claims 11 and 20:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester interface) functions to generate a series of pseudo random data words (test pattern generator) and is connected to the parallel data on data bus 21. Takinosawa also teaches The BIST analyzer circuit 49 (error detector), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25 (parallel data from SERDES), then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received. (Page 3, ¶ 28, Page 4, ¶ 31, Fig. 2).

Claims 12 and 18:

Takinosawa teaches that the USB physical layer 18 (SERDES) comprises a built-in self-test circuit (TX-BIST) circuit 35 (tester comprising a BIST state machine), a

multiplexer 36, a built-in self-test analyzer circuit 49 (plurality of testers) and is connected to the data bus 21 (test bus). (Page 2, ¶ 24, Fig. 2).

Claim 13:

Takinosawa teaches that data to be transmitted is provided by the microcontoller 12 (external device) to the USB link layer 16 (IOC) which functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 (FTI) via a data bus 21 (common test bus) as well as transmit control signals 23 (addressable commands). (Page 2, ¶ 22).

Claim 14:

Takinosawa teaches The USB link layer 16 (IOC) provides transmit control signals 23 to the USB physical layer 18 (FTI), which function as trigger signals indicating that the data transferred is valid and can be transmitted by the USB physical layer 18 (FTI) (IOC enabled to manipulate FTI).

Claim 16:

Takinosawa teaches that data to be transmitted is provided by the microcontoller 12 (external device) to the USB link layer 16 (input/output controller) which functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 via a data bus 21 (common test bus) as well as transmit control signals 23 (addressable commands). (Page 2, ¶ 22).

Claim 17:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester) functions (enabling all test interfaces) to generate a series of pseudo random

data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (test controller). Takinosawa also teaches The BIST analyzer circuit 49 (tester), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25, then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received (monitor performance of SERDES). (Page 3, ¶ 28, Page 4, ¶ 31).

Claim 19:

Takinosawa also discloses it is possible to conduct self test on two chips (e.g. two USB physical layers) (forming an insulative package). (Page 6, ¶ 48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa (US-2003/0035473), hereinafter Takinosawa in view of Lesea (US-2003/0023912), hereinafter Lesea.

Claim 1:

Takinosawa teaches the USB physical layer 18 functions to convert the parallel data received from the USB link layer 16 (core processing logic) into a serial format

(serializer) and converts the data to a parallel format (deserializer) and transmits the data to the USB link layer 16 via a data bus 25. Takinosawa also teaches the data to be transmitted is first provided by the microcontroller 12 to the USB link layer 16 (core processing logic), which operates at a lower clock rate (e.g., 30 MHz) as compared to the output data rate of the USB physical layer 18. Takinosawa further teaches the USB link layer 16 (core processing logic) functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 via a data bus 21 (common test bus). Takinosawa discloses that the USB physical layer 18 comprises a built-in self-test circuit (TX-BIST) circuit 35, a multiplexer 36, a built-in self-test analyzer circuit 49 (tester). (Page 2, ¶s 22-24, Figs. 1 and 2). Takinosawa does not explicitly teach "a plurality of SERDESs..." and a plurality of functionally identical testers...". However, Takinosawa does disclose that it is possible to conduct self-test on two chips (e.g. two USB physical layers) (plurality of SERDESs and testers). (Page 6, ¶ 48). Lesea suggests a plurality of SERDESs and functionally identical testers with a FPGA that includes sixteen built-in self-test SERDES circuits (plurality of SERDESs and testers) that are each capable of communicating at gigabit speeds. (Page 2, ¶s 23, 25, 27). Lesea also illustrates in Figure 1 that these sixteen built-in self-test SERDES circuits are integrated in the same integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takinosawa's the USB physical layer 18 (SERDES) to be configured according to Lesea's plurality of built-in self-test SERDES circuits (plurality of SERDESs and testers) on the same integrated circuit. The artisan would have been motivated to do so because this would

enable Takinosawa to test each USB physical layer 18 (SERDES) independently as well as saving area via the integration.

Claim 2:

Takinosawa teaches a peripheral device 10 (semiconductor substrate) comprises a microcontroller 12 (core processing logic), an application layer 14, a USB link layer 16 (core processing logic) and a USB physical layer 18 (SERDESs and testers). (Page 2, ¶ 20).

Claims 3:

Takinosawa further teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (functional test interface (FTI)) functions to generate a series of pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester controller). Takinosawa discloses that multiplexer 36 (tester controller) is controlled via the TX-BIST enable signal (select operational modes) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (tester interface) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2).

Claims 4:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester interface) functions to generate a series of pseudo random data words (test pattern generator) and is connected to the parallel data on data bus 21. Takinosawa also teaches The BIST analyzer circuit 49 (error detector), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the

bus 25 (parallel data from SERDES), then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received. (Page 3, ¶ 28, Page 4, ¶ 31, Fig. 2).

Claim 5:

Takinosawa teaches the USB link layer 16 (core processing logic) functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 (SERDESs) via a data bus 21 (common test bus).

Claims 6:

Takinosawa teaches that data to be transmitted is provided by the microcontoller 12 (external device) to the USB link layer 16 (input/output controller) which functions to provide data to be transmitted in a parallel format (e.g., 16 bit word) to the USB physical layer 18 via a data bus 21 (common test bus) as well as transmit control signals 23 (addressable commands). (Page 2, ¶ 22).

Claims 7:

Takinosawa teaches that the USB physical layer 18 (SERDES) comprises a built-in self-test circuit (TX-BIST) circuit 35 (tester comprising a BIST state machine), a multiplexer 36, a built-in self-test analyzer circuit 49 (plurality of testers) and is connected to the data bus 21 (test bus). (Page 2, ¶ 24, Fig. 2).

Claim 8:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester) functions (responsive to individual commands) to generate a series of pseudo random data words (individually but concurrently operated), which are output by

the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester). (Page 3, ¶ 28).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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